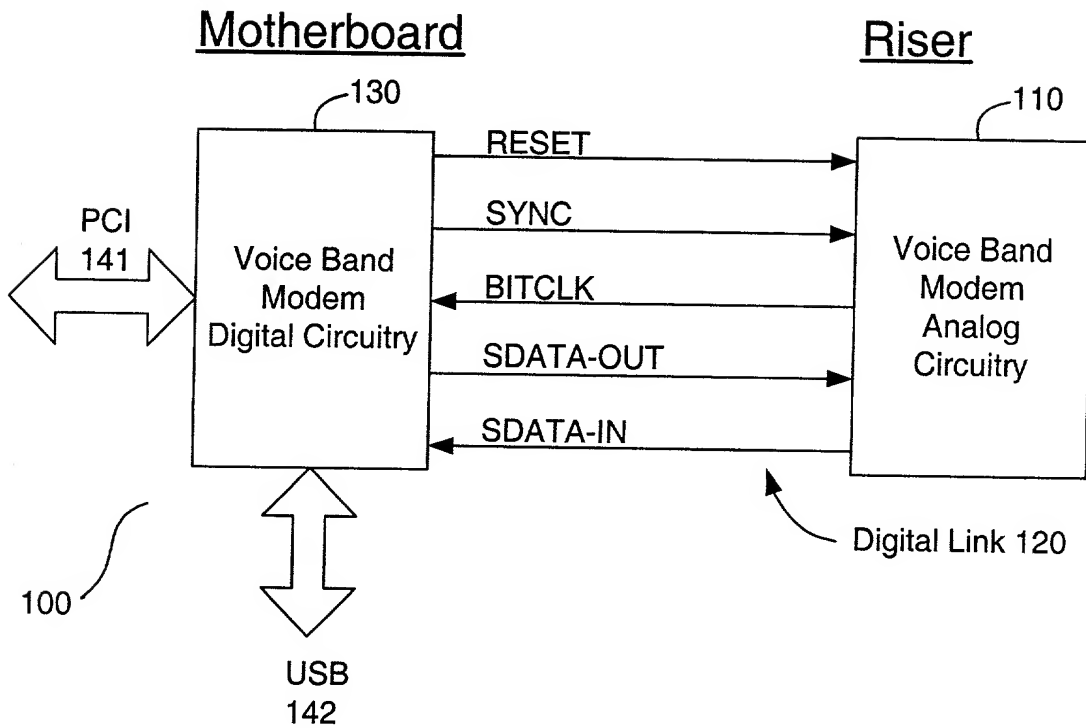


**Fig. 1A**  
(Prior Art)



**Fig. 1B**

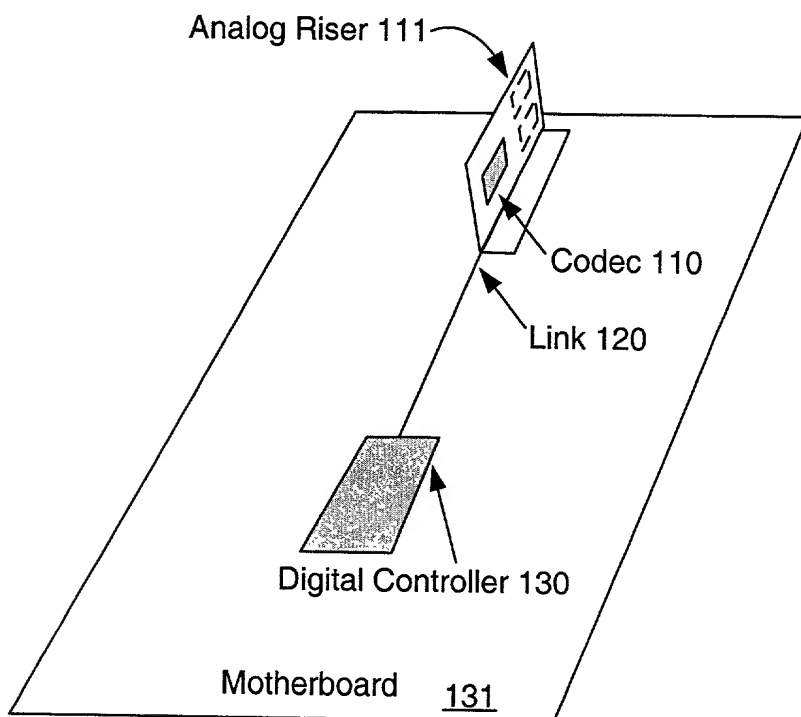


Fig. 2A

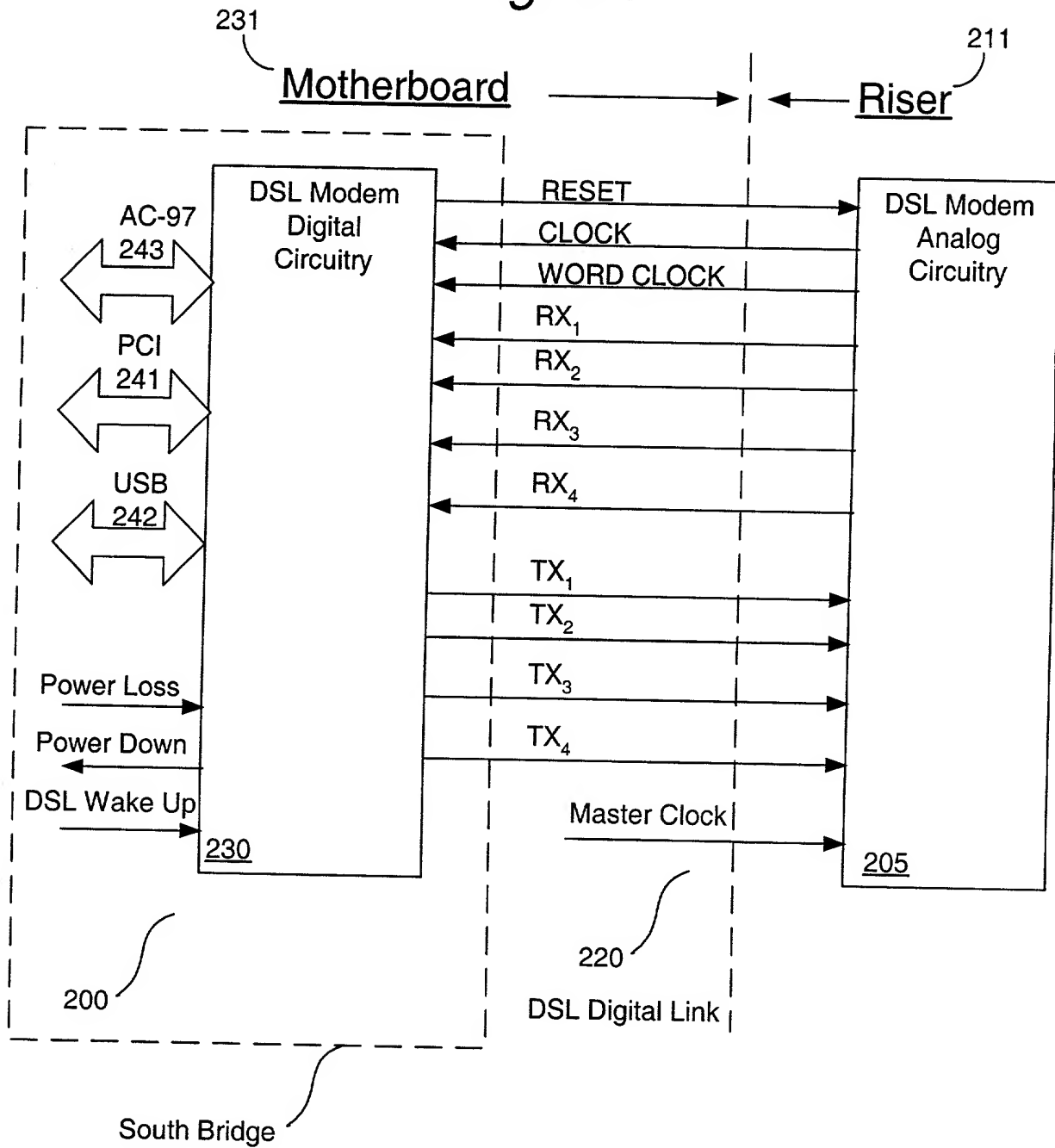


Fig. 2B-(Sheet 1)

Digital Section

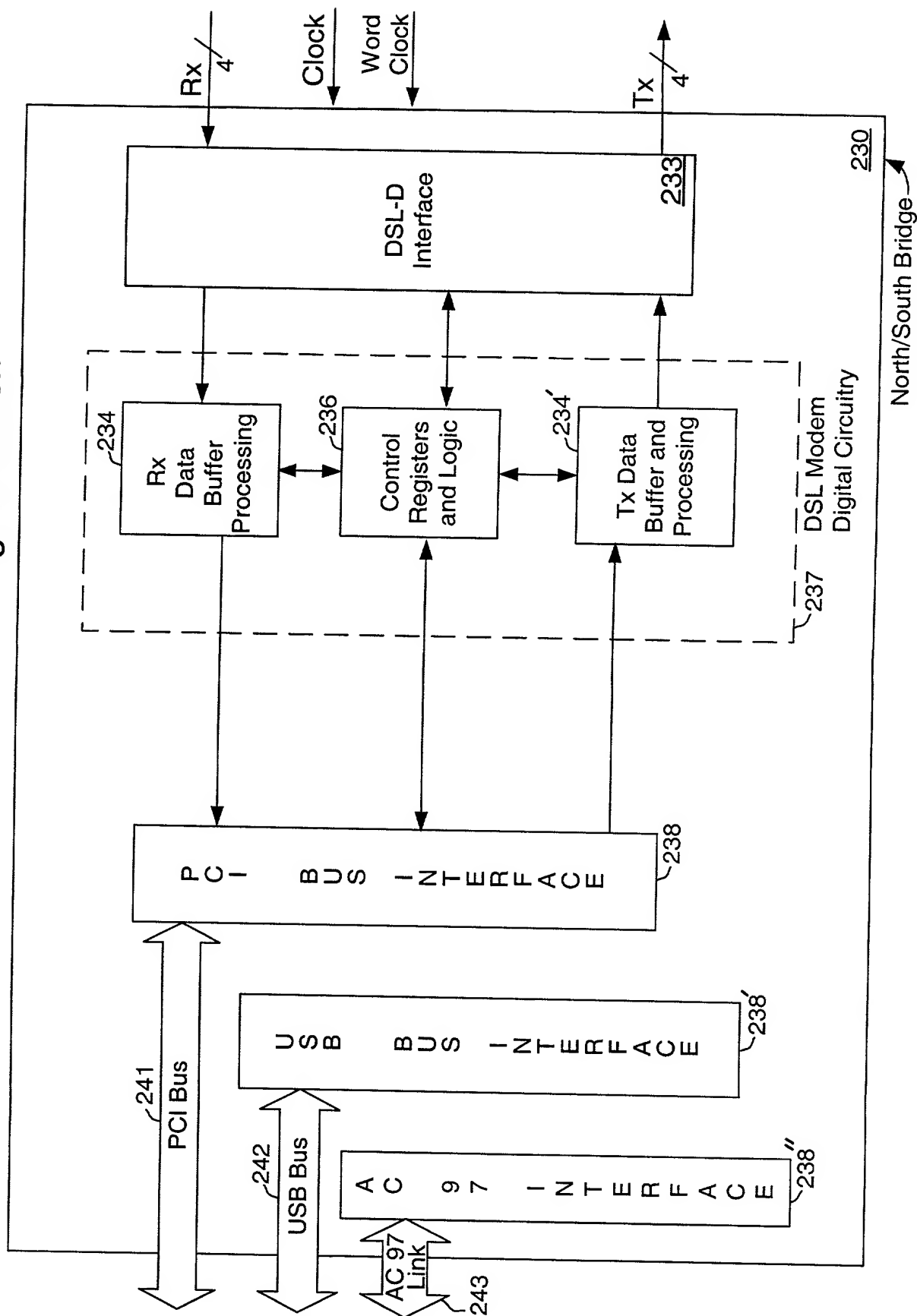


Fig. 2B-(Sheet 2)

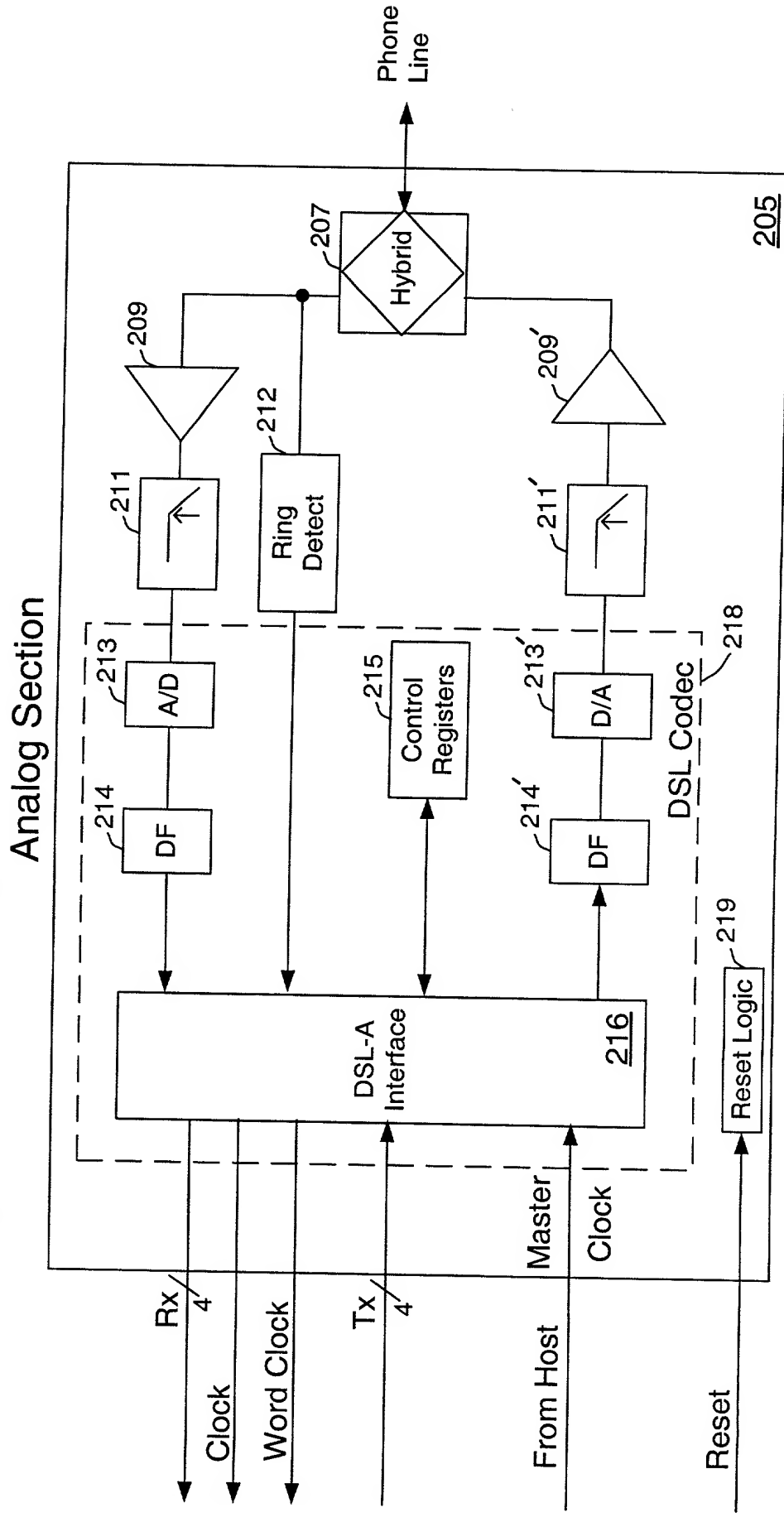




Fig. 4

DSL Link Pins	Cycle 1	Cycle 2	Cycle 3	Cycle 4
RxData[3:0]	Control, 0, RxClav, TxClav	RxSOC, RxAddr.[2:0]	RxData[7:4]	RxData[3:0]
TxData[3:0]	Control, 0, RxEnb, TxEnb	TxSOC, TxAddr.[2:0]	TxData[7:4]	TxData[3:0]